I claim:

1. A circuit for testing a data memory, comprising:

a processing unit connected to the data memory, said processing unit applying a first function to a predetermined test pattern for generating therefrom data items to be written to the data memory, said processing unit reading the data items from the data memory and applying a second function to the data items read from the data memory for generating therefrom test data items;

wherein the second function is a reciprocal function of the first function and a number of the data items is greater than a number of test data items; and

a test device connected to and outputting to said processing unit function data items defining the first function and the second function for said processing unit.

2. The circuit according to claim 1, wherein a number of the data items read from the data memory is greater than a number of the test data items generated therefrom.

3. The circuit according to claim 1, wherein a number of the data items generated from the test pattern for writing to the

data memory is greater than a number of the test data items forming the test pattern.

4. The circuit according to claim 1, which comprises a comparison device connected to said processing device and configured to determine from the test data items produced by said processing device from the stored data items read from the data memory whether the data memory is faulty.

5. The circuit according to claim 1, which comprises a buffer store connected between said processing unit and the data memory, for intermediately storing the data items produced from the test pattern data item and writing to the data memory.

6. The circuit according to claim 1, which comprises a buffer store connected between said processing unit and the data memory, for intermediately storing the data items read from the data memory and forwarding the data items for processing in said processing unit.

7. The circuit according to claim 1, which comprises a first buffer store connected between said processing unit and the data memory, for intermediately storing the data items produced from the test pattern data item and writing to the data memory, and a second buffer store connected between said

processing unit and the data memory, for intermediately storing the data items read from the data memory and forwarding the data items for processing in said processing unit.

8. The circuit according to claim 1 commonly integrated in a memory module together with the data memory.

9. A method of testing a data memory, which comprises the following steps:

receiving a predetermined test pattern data item;

processing the test pattern data item with a first function to produce data items for the data memory with a greater data width than the test pattern data item;

storing the data items in the data memory;

reading the stored data items from the data memory;

processing the stored data items with a second function being a reciprocal function of the first function, to produce test data items and to check a functionality of the data memory, and thereby defining the first function and the second function by function data items predetermined by a test device.

10. The method according to claim 9, which comprises comparing a plurality of the test data items with one another in order to detect any fault in the data memory.

11. The method according to claim 9, which comprises using the predetermined test pattern data item as a stored data item for the data memory.

12. The method according to claim 9, which comprises storing the data items at one address in the data memory.

13. The method according to claim 9, which comprises reading the stored data items from one address in the data memory.